CLAIMS

What is claimed is:

1. A capacitor array in an integrated circuit, the capacitor array comprising:

a plurality of dummy unit capacitor cells decoupled from signal paths to provide visual symmetry;

a plurality of active unit capacitor cells having a terminal coupled to signal paths carrying analog signals; and

wherein the plurality of active unit capacitor cells is arranged in the capacitor array with the dummy unit capacitor cells to provide visual symmetry and electrical symmetry.

2. The capacitor array of claim 1 wherein,

the electrical symmetry to provide electrical matching between active unit capacitor cells, and

the visual symmetry to provide process environment uniformity.

3. The capacitor array of claim 1 wherein,

the visual symmetry is provided by

selecting the same size and shape of capacitor plates for each unit capacitor in the capacitor array, and

uniformly spacing each unit capacitor in the capacitor array;

and wherein

the electrical symmetry is provided by

arranging the plurality of active unit capacitors amongst the plurality of dummy unit capacitors in the

capacitor array so that the far range fringing fields are symmetric.

4. A capacitor array in an integrated circuit, the capacitor array comprising:

a plurality of unit capacitor cells arranged to provide visual symmetry;

a set of N active unit capacitor cells of the plurality of unit capacitor cells having a terminal coupled to a signal path to carry analog signals;

if N is a prime number, arranging the N active unit capacitor cells to be symmetrically located to form an N-equilateral two-dimensional shape to provide electrical symmetry,

otherwise if N is not a prime number,

dividing the set of N active unit capacitor cells into P subsets of M active unit capacitor cells, arranging the M active unit capacitor cells of each of the P subsets to be symmetrically located to form an M-equilateral two-dimensional shape in a neighborhood, and

separating each neighborhood of each M-equilateral two-dimensional shape by one or more dummy unit capacitor cells to avoid encroachment of one neighborhood into another in order to provide electrical symmetry.

5. The capacitor array of claim 4 wherein,

the plurality of unit capacitor cells are arranged in equally spaced apart rows and columns to provide visual symmetry.

6. The capacitor array of claim 4 wherein,
the electrical symmetry to provide electrical matching between active unit capacitor cells, and
the visual symmetry to provide process environment uniformity.

7. The capacitor array of claim 4 wherein,
the N-equilateral shape is slightly skewed, and
a predetermined distance of separation is maintained between active cells.

8. The capacitor array of claim 4 wherein,
the unit capacitor cells are integrated circuit capacitors.

9. The capacitor array of claim 8 wherein,
the integrated circuit capacitors are metal oxide semiconductor capacitors.

10. The capacitor array of claim 8 wherein,
the integrated circuit capacitors are thin film capacitors.

11. A method in an integrated circuit comprising:
arranging a plurality of dummy unit capacitors and a plurality of active unit capacitors in a capacitor array to provide visual symmetry;

further arranging the plurality of dummy unit capacitors and the plurality of active capacitors in the capacitor array to provide electrical symmetry;

wherein the dummy unit capacitors are decoupled from signal paths; and

wherein the active unit capacitors have at least one terminal coupled to a signal path carrying an analog signal.

12. The method of claim 11 wherein,

the electrical symmetry to provide electrical matching between active unit capacitors, and

the visual symmetry to provide process environment uniformity.

13. The method of claim 11 wherein,

the visual symmetry is provided by

selecting the same size and shape of capacitor plates for each unit capacitor in the capacitor array, and

uniformly spacing each unit capacitor in the capacitor array.

14. The method of claim 11 wherein,

the electrical symmetry is provided by

arranging the plurality of active unit capacitors amongst the plurality of dummy unit capacitors in the capacitor array so that the far range fringing fields are symmetric.

15. The method of claim 11 wherein,

the method is a layout method defining mask layers for the manufacture of a capacitor array in the integrated circuit.

16. A computer program product for layout of a capacitor array in an integrated circuit, comprising:

a computer usable medium having

computer readable program code to arrange a plurality of dummy unit capacitors and a plurality of active unit capacitors in a capacitor array to provide visual symmetry, and

computer readable program code to arrange the plurality of active capacitors amongst the plurality of dummy unit capacitors in the capacitor array to provide symmetric far range fringing fields to each of the plurality of active capacitors;

and

wherein the dummy unit capacitors are decoupled from signal paths and the active unit capacitors have at least one terminal coupled to a signal path carrying an analog signal.

17. The computer program product of claim 16 wherein,

the visual symmetry is provided by

selecting the same size and shape of capacitor plates for each unit capacitor in the capacitor array, and

uniformly spacing each unit capacitor in the capacitor array.

18. The computer program product of claim 16 wherein,

the computer usable medium further has

computer readable program code to define the mask layers of a unit capacitor of the capacitor array.

19. The computer program product of claim 16 wherein,

the computer usable medium is a semiconductor medium, a magnetic medium, an optical medium, or a processor readable medium.

20. The computer program product of claim 16 wherein,

the computer usable medium is a computer data signal embodied in a carrier wave over a transmission medium.

21. An N-bit digital to analog converter (DAC) with a binary-weighted capacitor ladder in an integrated circuit, the N-bit DAC comprising:

N-1 sampling switches each having a control gate, a first pole, and a second pole coupled to a voltage reference;

a switch controller to receive an N-bit digital data input signal and generate N-1 control signals, the N-1 control signals respectfully coupled to each control gate of the N-1 sampling switches to switch the N-1 sampling switches open and closed in response to the N-bit digital data input signal;

N capacitors formed out of a plurality of active unit capacitor cells in a capacitor array, each of the N capacitors having a top capacitor plate coupled together and to an output of the binary-weighted capacitor ladder, one of the N capacitors having a bottom capacitor plate coupled to a ground while the remaining N-1 capacitors have a bottom capacitor plate respectively coupled to each first pole of the N-1 sampling switches; and

wherein the plurality of active unit capacitor cells to form the N capacitors being arranged with a plurality of dummy unit capacitor cells in the capacitor array to provide visual symmetry and electrical symmetry.

22. The N-bit DAC of claim 21 wherein,
the integrated circuit is a digital to analog converter.

23. The N-bit DAC of claim 21 wherein,
the integrated circuit is an analog to digital converter and the N-bit DAC is a portion of each stage of the analog to digital converter to successively approximate the analog input signal.

24. The N-bit DAC of claim 21 wherein
the electrical symmetry to provide electrical matching between active unit capacitors, and
the visual symmetry to provide process environment uniformity.

25. The N-bit DAC of claim 21 wherein
the visual symmetry is provided by
selecting the same size and shape of capacitor plates for each unit capacitor in the capacitor array, and
uniformly spacing each unit capacitor in the capacitor array.

26. The N-bit DAC of claim 21 wherein

the electrical symmetry is provided by

arranging the plurality of active unit capacitors amongst the plurality of dummy unit capacitors in the capacitor array so that the far range fringing fields are symmetric.

27. The N-bit DAC of claim 21 wherein

the electrical symmetry is provided by

if a number M of active unit capacitor cells forming the capacitor is a prime number, arranging the M active unit capacitor cells to be symmetrically located to form an M-equilateral two dimensional shape to provide electrical symmetry,

otherwise if M is not a prime number,

dividing the set of M active unit capacitor cells into P subsets of Q active unit capacitor cells, arranging the Q active unit capacitor cells of each of the P subsets to be symmetrically located to form an Q-equilateral two dimensional shape in a neighborhood, and

separating each neighborhood of each Q-equilateral two-dimensional shape by one or more dummy unit capacitor cells to avoid encroachment of one neighborhood into another.

28. The N-bit DAC of claim 21 further comprising:

N grounding switches each having a control gate, a first pole, and a second pole coupled to the ground;

and

wherein one of the N grounding switches has the first pole coupled to the output;

wherein the remaining N-1 capacitors have their bottom capacitor plate respectively coupled to each first pole of the remaining N-1 grounding switches; and

wherein the switch controller to further generate N inverted control signals, the N inverted control signals respectfully coupled to each control gate of the N grounding switches to switch the N grounding switches open and closed in response to the N-bit digital data input signal.

29. An N-bit digital to analog converter (DAC) with an equally-weighted capacitor array in an integrated circuit, the N-bit DAC comprising:

a first plurality of N switches each having a switch control gate, a first pole, and a second pole, the second pole of each of the first plurality of N switches coupled to a low level voltage supply;

a second plurality of N switches each having a switch control gate, a first pole, and a second pole, the second pole of each of the second plurality of N switches coupled to a voltage reference, the first pole of each of the second plurality of N switches coupled respectively to the corresponding first pole of the first plurality of N switches;

a digital input signal having N control signals, each of the N control signals coupled respectively to each switch control gate of the first plurality of N switches and coupled respectively to each switch control gate of the second plurality of N switches, the N control signals to switch the second plurality of N switches open and closed and to switch the first plurality of N switches closed and open, respectively, in response to the digital input signal;

N capacitors formed out of a plurality of active unit capacitor cells in a capacitor array, each of the N capacitors having a top capacitor plate coupled together and to an analog output of the DAC, the N capacitors each have a bottom capacitor plate respectively coupled to each first pole of the first plurality of N switches and each first pole of the second plurality of N switches; and

wherein the plurality of active unit capacitor cells to form the N capacitors being arranged with a plurality of dummy unit capacitor cells in the capacitor array to provide visual symmetry and electrical symmetry to provide a substantial equally matched capacitance for each of the N capacitors.

30. The N-bit DAC of claim 29 wherein,

the integrated circuit is a digital to analog converter.

31. The N-bit DAC of claim 29 wherein,

the integrated circuit is an analog to digital converter and the N-bit DAC is a portion of each stage of the analog to digital converter to successively approximate the analog input signal.

32. The N-bit DAC of claim 29 wherein

the electrical symmetry to provide electrical matching between active unit capacitors, and

the visual symmetry to provide process environment uniformity.

33. The N-bit DAC of claim 29 wherein

the visual symmetry is provided by

selecting the same size and shape of capacitor plates for each unit capacitor in the capacitor array, and

uniformly spacing each unit capacitor in the capacitor array.

34. The N-bit DAC of claim 29 wherein

the electrical symmetry is provided by

arranging the plurality of active unit capacitors amongst the plurality of dummy unit capacitors in the capacitor array so that the far range fringing fields are symmetric.

35. The N-bit DAC of claim 29 wherein

the electrical symmetry is provided by

if a number M of active unit capacitor cells forming the capacitor is a prime number, arranging the M active unit capacitor cells to be symmetrically located to form an M-equilateral two dimensional shape to provide electrical symmetry,

otherwise if M is not a prime number,

dividing the set of M active unit capacitor cells into P subsets of Q active unit capacitor cells, arranging the Q active unit capacitor cells of each of the P subsets to be symmetrically located to form an Q-equilateral two dimensional shape in a neighborhood, and

separating each neighborhood of each Q-equilateral two-dimensional shape by one or more dummy unit capacitor cells to avoid encroachment of one neighborhood into another.

36. The N-bit DAC of claim 29 wherein
the first plurality of N switches are n-channel field effect transistors; and
the second plurality of N switches are p-channel field effect transistors.

37. The N-bit DAC of claim 36 wherein
the digital input signal is a thermometer coded digital input signal, and
each of the N control signals are directly coupled respectively to each switch control gate of the n-channel field effect transistors and are directly coupled respectively to each switch control gate of the p-channel field effect transistors.

38. The N-bit DAC of claim 29 wherein
the N control signals include N positive control signals and N negative control signals,
each of the N positive control signals are directly coupled respectively to each switch control gate of the first plurality of N switches, and
each of the N negative control signals are directly coupled respectively to each switch control gate of the second plurality of N switches.

39. The N-bit DAC of claim 38 wherein
the N negative control signals are respective inverted logical signals of the N positive control signals.

40. The N-bit DAC of claim 29 further comprising:
a switch controller to receive the digital input signal and generate the N control signals in response thereto.

41. The N-bit DAC of claim 40 wherein
the N control signals include N positive control signals and N negative control signals,
each of the N positive control signals are directly coupled respectively to each switch control gate of the first plurality of N switches, and
each of the N negative control signals are directly coupled respectively to each switch control gate of the second plurality of N switches.

42. The N-bit DAC of claim 41 wherein
the N negative control signals are respective inverted logical signals of the N positive control signals.

43. A pipelined analog to digital converter (ADC) in an integrated circuit to receive an analog input signal and to generate a digital output signal, the pipelined analog to digital converter (ADC) comprising:
a plurality of M converter stages coupled in series together, each of the M converter stages to receive an analog input and generate an analog residue output, each of the plurality of M converter stages including
a K-bit flash analog to digital converter to receive the analog input and generate a stage digital output,

wherein K is a variable from stage to stage over the plurality of M converter stages;

an N-bit digital to analog converter (DAC) with an equally-weighted capacitor array, the N-bit DAC to receive the stage digital output to generate an estimated analog output, the N-bit DAC including

a first plurality of N switches each having a switch control gate, a first pole, and a second pole, the second pole of each of the first plurality of N switches coupled to a first voltage reference,

a second plurality of N switches each having a switch control gate, a first pole, and a second pole, the second pole of each of the second plurality of N switches coupled to a second voltage reference, the first pole of each of the second plurality of N switches coupled respectively to the corresponding first pole of the first plurality of N switches,

wherein the stage digital output has N control signals, each of the N control signals coupled respectively to each switch control gate of the first plurality of N switches and coupled respectively to each switch control gate of the second plurality of N switches, the N control signals to switch the second plurality of N switches open and closed and to switch the first plurality of N switches closed and open, respectively, in response to the stage digital output,

N capacitors formed out of a plurality of active unit capacitor cells in a capacitor array, each of the N capacitors having a top capacitor plate coupled together and to the estimated analog output, the N capacitors each have a bottom capacitor plate respectively coupled to each first pole of the first plurality of N switches and each first pole of the

second plurality of N switches,

wherein the plurality of active unit capacitor cells to form the N capacitors being arranged with a plurality of dummy unit capacitor cells in the capacitor array to provide visual symmetry and electrical symmetry to provide a substantial equally matched capacitance for each of the N capacitors, and

wherein N is a variable from stage to stage over the plurality of M converter stages;

and,

an analog subtractor to receive the analog input and subtract the estimated analog output therefrom to generate the analog residue output.

44. The pipelined analog to digital converter (ADC) of claim 43 wherein

the analog subtractor includes an amplifier to amplify the magnitude of analog residue output.

45. The pipelined analog to digital converter (ADC) of claim 43 wherein

a first converter stage of the plurality of M converter stages to receive the analog input signal of the analog to digital converter (ADC) as the analog input,

and the analog to digital converter (ADC) further includes

a digital bit corrector to receive each stage digital output of the respective plurality of M converter stages and to generate the digital output signal of the analog to digital converter in response to the analog input signal.

46. The pipelined analog to digital converter (ADC) of claim 43 further comprising:

a last converter stage coupled in series with an Mth converter stage of the plurality of M converter stages, the last converter stage including

an J-bit flash analog to digital converter to receive the analog residue output of the Mth converter stage as the analog input and generate a last stage digital output.

47. The pipelined analog to digital converter (ADC) of claim 46 wherein

a first converter stage of the plurality of M converter stages to receive the analog input signal of the analog to digital converter (ADC) as the analog input,

and the analog to digital converter (ADC) further includes

a digital bit corrector to receive each stage digital output of the respective plurality of M converter stages and the last stage digital output of the last converter stage to generate the digital output signal of the analog to digital converter in response to the analog input signal.

48. The pipelined analog to digital converter (ADC) of claim 43 wherein

the N-bit DAC in each of the plurality of M converter stages further includes

a switch controller to receive the digital input signal and generate the N control signals in response thereto.

49. The pipelined analog to digital converter (ADC) of claim 43 wherein
the first voltage reference is a negative voltage reference and
the second voltage reference is a positive voltage reference.

50. The pipelined analog to digital converter (ADC) of claim 43 wherein
the first voltage reference is a low level voltage supply.

51. The pipelined analog to digital converter (ADC) of claim 43 wherein
the low level voltage supply is ground.

52. The pipelined analog to digital converter (ADC) of claim 43 wherein
the N-bit DAC in each of the plurality of M converter stages further includes
a third plurality of N switches each having a switch control gate, a first pole, and a second pole, the second pole of each of the second plurality of N switches coupled to a low level voltage supply, the first pole of each of the third plurality of N switches coupled respectively to the corresponding first pole of the first plurality of N switches.

53. The pipelined analog to digital converter (ADC) of claim 52 wherein

the switch control gates of the third plurality of switches are coupled together and to a reset control signal to close each of the third plurality of switches and initialize the N capacitors of the capacitor array.

54. A pipelined analog to digital converter (ADC) in an integrated circuit to receive an analog input signal and to generate a digital output signal, the pipelined analog to digital converter (ADC) comprising:

a plurality of converter stages coupled in series together, each of the plurality of converter stages including

a flash analog to digital converter to receive the analog input and generate a stage digital output;

a digital to analog converter (DAC) with a capacitor array, the digital to analog converter to receive the stage digital output to generate an estimated analog output, the digital to analog converter including

a plurality of switches each having a switch control gate, a first pole, and a second pole,

a plurality of active unit capacitor cells in the capacitor array, each of the active unit capacitor cells having a capacitor plate coupled to each respective first pole of the plurality of switches, respectively,

wherein the plurality of active unit capacitor cells to form the active capacitors being arranged with a plurality of dummy unit capacitor cells in the

capacitor array to provide visual symmetry and electrical symmetry to provide a substantial equally matched capacitance for each of the active unit capacitors.

55. The pipelined analog to digital converter (ADC) of claim 54 wherein

the electrical symmetry to provide electrical matching between active unit capacitors, and

the visual symmetry to provide process environment uniformity.

56. The pipelined analog to digital converter (ADC) of claim 54 wherein

the visual symmetry is provided by

selecting the same size and shape of capacitor plates for each unit capacitor in the capacitor array, and

uniformly spacing each unit capacitor in the capacitor array.

57. The pipelined analog to digital converter (ADC) of claim 54 wherein

the electrical symmetry is provided by

arranging the plurality of active unit capacitors amongst the plurality of dummy unit capacitors in the capacitor array so that the far range fringing fields are symmetric.

58. The pipelined analog to digital converter (ADC) of claim 54 wherein

the electrical symmetry is provided by

if a number M of active unit capacitor cells forming the active capacitor is a prime number, arranging the M active unit capacitor cells to be symmetrically located to form an M-equilateral two dimensional shape to provide electrical symmetry,

otherwise if M is not a prime number,

dividing the set of M active unit capacitor cells into P subsets of Q active unit capacitor cells, arranging the Q active unit capacitor cells of each of the P subsets to be symmetrically located to form an Q-equilateral two dimensional shape in a neighborhood, and

separating each neighborhood of each Q-equilateral two-dimensional shape by one or more dummy unit capacitor cells to avoid encroachment of one neighborhood into another.

59. The pipelined analog to digital converter (ADC) of claim 54 wherein

a bottom capacitor plate is the capacitor plate of each of the active capacitors which is coupled to each respective first pole of the plurality of switches.

60. A pipelined analog to digital converter (ADC) in an integrated circuit to receive an analog input signal and to generate a digital output signal, the pipelined analog to digital converter (ADC) comprising:

a plurality of converter stages coupled in series together, each of the plurality of converter stages including

a flash analog to digital converter to receive the analog input and generate a stage digital output;

a multiplying digital to analog converter (MDAC) with a capacitor array, the digital to analog converter to receive the stage digital output to generate a residual analog output, the multiplying digital to analog converter including

a first plurality of switches each having a switch control gate, a first pole, and a second pole, the second pole of each of the first plurality of switches coupled together and to a negative reference voltage,

a second plurality of switches each having a switch control gate, a first pole, and a second pole, the second pole of each of the second plurality of switches coupled together and to a positive reference voltage, each first pole of the second plurality of switches correspondingly coupled to each first pole of the first plurality of switches, respectively.

a third plurality of switches each having a switch control gate, a first pole, and a second pole, each second pole of the third plurality of switches corresponding coupled to each first pole of the first plurality of switches and each first pole of the second plurality of switches, respectively,

a fourth plurality of switches each having a switch control gate, a first pole, and a second pole, the second pole of each of the fourth plurality of switches coupled together and to an analog input,

a plurality of active capacitors in the capacitor array each having a first capacitor plate and a second

capacitor plate, each first capacitor plate of the active capacitors coupled to each first pole of the third plurality of switches and each first pole of the fourth plurality of switches, respectively, each second capacitor plate of each of the active capacitors coupled together,

an operational amplifier having an input coupled to each second capacitor plate of each of the active capacitors, the operational amplifier to generate the analog residue output,

a switch having a switch control gate, a first pole, and a second pole, the first pole of the switch coupled to input of the operational amplifier and the second capacitor plate of each of the active capacitors, the second pole of the switch coupled to the analog residue output of the operational amplifier, and

wherein a plurality of active unit capacitor cells form the active capacitors and are arranged with a plurality of dummy unit capacitor cells in the capacitor array to provide visual symmetry and electrical symmetry to provide a substantial equally matched capacitance for each of the active capacitors.

61. The pipelined analog to digital converter (ADC) of claim 60 wherein

the multiplying digital to analog converter further includes

a fifth plurality of switches each having a switch control gate, a first pole, and a second pole, the second pole of each of the fifth plurality of switches coupled together and to a low level power

supply voltage, each first pole of the fifth plurality of switches correspondingly coupled to each first pole of the first plurality of switches and to each first pole of the second plurality of switches, respectively.

62. The pipelined analog to digital converter (ADC) of claim 61 wherein

the low level power supply voltage is ground.

63. The pipelined analog to digital converter (ADC) of claim 61 wherein

the multiplying digital to analog converter further includes

a sixth plurality of switches each having a switch control gate, a first pole, and a second pole, the second pole of each of the sixth plurality of switches coupled together and to the analog residue output, each first pole of each of the sixth plurality of switches coupled to each first capacitor plate of the active capacitors, each first pole of the third plurality of switches, and each first pole of the fourth plurality of switches, respectively.

64. The pipelined analog to digital converter (ADC) of claim 60 wherein

the electrical symmetry to provide electrical matching between active unit capacitors, and

the visual symmetry to provide process environment uniformity.

65. The pipelined analog to digital converter (ADC) of claim 60 wherein
the visual symmetry is provided by
selecting the same size and shape of capacitor plates for each unit capacitor in the capacitor array, and
uniformly spacing each unit capacitor in the capacitor array.

66. The pipelined analog to digital converter (ADC) of claim 60 wherein
the electrical symmetry is provided by
arranging the plurality of active unit capacitors amongst the plurality of dummy unit capacitors in the capacitor array so that the far range fringing fields are symmetric.

67. The pipelined analog to digital converter (ADC) of claim 60 wherein
the electrical symmetry is provided by
if a number M of active unit capacitor cells forming the active capacitor is a prime number, arranging the M active unit capacitor cells to be symmetrically located to form an M-equilateral two dimensional shape to provide electrical symmetry,
otherwise if M is not a prime number,
dividing the set of M active unit capacitor cells into P subsets of Q active unit capacitor cells, arranging the Q active unit capacitor cells of each of the P subsets to be

symmetrically located to form an Q-equilateral two dimensional shape in a neighborhood, and

separating each neighborhood of each Q-equilateral two-dimensional shape by one or more dummy unit capacitor cells to avoid encroachment of one neighborhood into another.